

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (original): Processor program product (1) to be run via a processor-system (80) for generating and/or analysing traffic signals for testing at least a part of at least one integrated-circuit-environment (8), which integrated-circuit-environment (8) is designed to handle traffic signals,

characterised in that said integrated-circuit-environment (8) comprises said processor-system (80), with said processor program product (1) comprising at least one generic module (2,3) and at least one specific module (4,5), with at least one specific module (4,5) being designed for interfacing said computer program product (1) with a protocol used in said integrated-circuit-environment (8).

2. (original): Processor program product (1) according to claim 1, characterised in that said processor-system (80) comprises at least one host processor (80), with generated traffic signals flowing from said host processor (80) to a buffer (87) and from said buffer (87) to at least one further circuit (83,84,85) of said integrated-circuit-environment (8).

3. (original): Processor program product (1) according to claim 2,

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characterised in that generated traffic signals leave said processor program product (1) via a software traffic sender (6), with traffic signals to be analysed arriving at said processor program product (1) via a software traffic receiver (7).

4. (currently amended): Processor program product (1) according to ~~claim 1, 2 or 3,~~claim 1,

characterised in that said protocol comprises a traffic protocol.

5. (original): Processor program product (1) according to claim 4,
characterised in that said traffic protocol comprises an Internet-Protocol or an Asynchronous-Transfer-Mode-Protocol or an Ethernet-protocol.

6. (currently amended): Processor program product (1) according to ~~claim 1, 2, 3, 4 or 5,~~claim 1,

characterised in that said protocol comprises a bus protocol.

7. (original): Processor program product (1) according to claim 6,
characterised in that said bus protocol comprises a flexbus4 protocol or a SPI4.2 protocol.

8. (original): Processor-system (80) for running a processor program product (1) for generating and/or analysing traffic signals for testing at least a part of at least one integrated-

circuit-environment (8), which integrated-circuit-environment (8) is designed to handle traffic signals,

characterised in that said integrated-circuit-environment (8) comprises said processor-system (80), with said processor program product (1) comprising at least one generic module (2,3) and at least one specific module (4,5), with at least one specific module (4,5) being designed for interfacing said computer program product (1) with a protocol used in said integrated-circuit-environment (8).

9. (original): Integrated-circuit-environment (8) to be tested via a processor-system (80) for running a processor program product (1) for generating and/or analysing traffic signals for testing at least a part of said integrated-circuit-environment (8), which integrated-circuit-environment (8) is designed to handle traffic signals,

characterised in that said integrated-circuit-environment (8) comprises said processor-system (80), with said processor program product (1) comprising at least one generic module (2,3) and at least one specific module (4,5), with at least one specific module (4,5) being designed for interfacing said computer program product (1) with a protocol used in said integrated-circuit-environment (8).

10. (original): Method for generating and/or analysing traffic signals via a processor-system (80) for testing at least a part of at least one integrated-circuit-environment (8) designed to handle traffic signals,

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characterised in that said integrated-circuit-environment (8) comprises said processor-system (80), with said method comprising at least one generic step and at least one specific step, with at least one specific step being performed for interfacing with a protocol used in said integrated-circuit-environment (8).